Press Release

IMMEDIATE RELEASE

CEA Demonstrates First Dynamically Routed Electro-Optical Router for Photonic Interposers

ISSCC 2026 Presentation Shows a 28 nm CMOS Router Achieving 18 ns Frame-Level Optical Path Setup

SAN FRANCISCO — Feb. 18, 2026 — Researchers from CEA-List and CEA-Leti today unveiled at ISSCC the first electro-optical router with dynamic, frame-level optical routing integrated with CMOS control logic, marking a major step toward practical optical networking inside advanced chiplet-based packages.

Their paper, **"A 3.19pJ/bit Electro-Optical Router with 18ns Setup Frame-Level Routing and 1-6 Wavelength Flexible Link Capacity for Photonic Interposers"**, demonstrates an electro-optical router implemented in 28 nm CMOS on a photonic interposer, capable of establishing optical paths in 18 nanoseconds. It dynamically selects one-to-six wavelengths per link, and achieves an energy efficiency of 3.19 pJ/bit with an active area of just 0.007 mm² per link.

Moving Optical Links Beyond Static Point-to-Point

Today's optical interconnects are largely limited to static, point-to-point links, with initialization and training times ranging from microseconds to milliseconds. While suitable for board-level or rack-scale communication, those latencies prevent optical links from being used as a true networking fabric inside multi-die packages.

The router addresses this gap by integrating optical switching, routing control, serializer/deserializer (SerDes), and clocking logic directly with silicon photonics. The result is a dynamically routed optical interconnect that operates at nanosecond timescales, enabling optical communication across centimeter-scale interposers with responsiveness previously limited to short electrical links.

It supports frame-level routing, allowing optical paths to be established and torn down on demand, and adjusts link capacity dynamically by selecting between one and six wavelengths, according to application needs. This flexibility enables efficient use of optical bandwidth, while maintaining ultra-low latency.

Architecture and Implementation

The prototype is fabricated in a 28 nm CMOS process and integrated on a photonic interposer. Compact analog drivers, combined with standard-cell-based SerDes and clocking circuits, enable dense integration of optical endpoints close to compute and memory resources.

While the architectural target includes CPUs, GPUs, and high-bandwidth memory (HBM) in large 2.5D and 3D packages, the current chip serves as a proof of concept, demonstrated on a small-scale multi-die system derived from CEA-Leti's earlier INTACT active interposer architecture (ISSCC 2020).

A First Integrated Dynamic Optical Routing

This is the first demonstration of dynamic optical routing in an integrated photonic switch that includes CMOS logic up to the protocol level. Previous optical switch demonstrations typically rely on standalone photonic devices with static or slowly reconfigured paths and do not integrate the full driving, control, and routing logic required for packet-level operation.

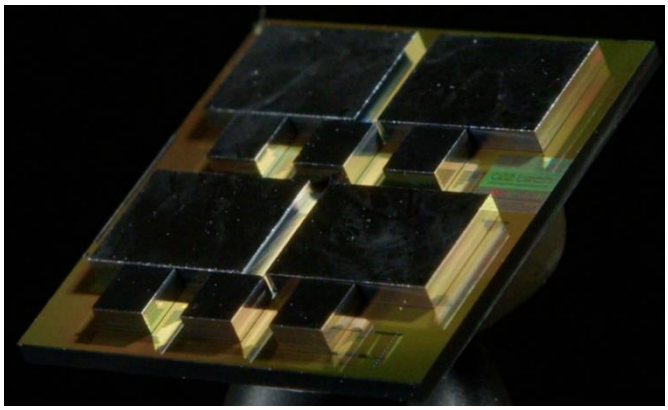
In contrast, the router operates as a miniature network switch inside the package, combining microring-based photonic devices with digital control logic to move data efficiently across the interposer. Compared with electrical routing fabrics or active interposers, the approach avoids power and latency penalties that scale with distance, relaxing constraints on data locality and enabling more flexible hardware architectures and software data placement.

Enabling New Chiplet Architectures

By bringing dynamic, ultra-low-latency optical networking into the package, the technology opens new possibilities for high-performance computing, AI accelerators, and data-intensive systems, where growing model sizes and memory demands increasingly stress conventional interconnects.

Rather than forcing all data to reside near compute cores to minimize electrical routing costs, dynamically routed optical links allow architects to treat memory and compute resources across the interposer as part of a unified, high-reach fabric without sacrificing latency or energy efficiency.

“As chiplet systems continue to grow in scale and complexity, the ability to move data efficiently across the entire package becomes essential,” said CEA-List’s Yvain Thonnart, lead author of the paper. “Our goal was to demonstrate that photonic links can provide that reach without sacrificing the flexibility designers expect from modern interconnects. This router is a step toward practical, dynamically routed optical networks that fit within standard CMOS design flows and real product constraints.”



Detail view of the system-on-interposer, with a companion electro-optical router for each computing die and two additional routers for primary IO. Light coupling to the optical network on interposer is achieved on fiber coupling visible on the bottom-right corner.

Photo Credit: KAM productions

About CEA-List (France)

Located in the innovation hubs of Paris-Saclay and Grenoble, CEA-List is a leading CEA technological research institute specializing in smart digital systems. Our 1,000 researchers and exeprts drive R&D programs, from advanced computing architectures, intelligent machines, digital instrumentation to data and systems engineering, designed to integrate AI and the digital thread into industry. By delivering disruptive technologies, we empower our industrial partners to boost their competitiveness while tackling major socio-economic challenges with a focus on human-centric and sustainable innovation. Committed to social and environmental responsibility, CEA-List has held the Institut Carnot label since 2006, reflecting our excellence in partnership-based research.
For more information: list.cea.fr | Linkedin

About CEA-Leti (France)

CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti pioneers micro-& nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 2,000 talents, a portfolio of 3,200 patents, 14,000 sq. meters of cleanroom space and a clear IP policy, the institute is based in Grenoble (France) and has offices in San Francisco (United States), Brussels (Belgium), Tokyo (Japan), Seoul (South Korea) and Taipei (Taiwan). CEA-Leti has launched 80 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

Technological expertise

CEA has a key role in transferring scientific knowledge and innovation from research to industry. This high-level technological research is carried out in particular in electronic and integrated systems, from microscale to nanoscale. It has a wide range of industrial applications in the fields of transport, health, safety and telecommunications, contributing to the creation of high-quality and competitive products.

For more information: www.cea.fr/english

Press Contacts

Sarah-Lyle Dampoux
sldampoux@mahoneylyle.com
+33 6 74 93 23 47